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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,437	07/26/2001	Sang Hoo Dhong	AUS9-2001-0301US1	7370

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
05/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/915,437	DHONG ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to restriction requirement file on 01/26/07. The examiner withdraws the restriction requirement file on 01/26/07.

Claims 1-18 remain pending in the application.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 1 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The recited limitations "defining a logic synthesis block comprising a dynamic logic circuit' and "eliminating unused devices in the intermediate circuit to produce a final circuit" and "sizing the devices in the final circuit" are just abstract ideas. The claim limitations do not specifically disclose what the input receiving and how to use the process. Thus the claim invention has no concrete result.

Claim 8 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The recited limitations "defining a logic synthesis block comprising a dynamic logic circuit' is just abstract ideas. The claim limitations do not specifically disclose what the input receiving and how to use the process. Thus the claim invention has no concrete result.

Claim 13 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The recited limitations "defining a logic synthesis block comprising a dynamic logic circuit' and "constraining the logic synthesis tool to the logic synthesis block" are

just abstract ideas. The claim limitations do not specifically disclose what the input receiving and how to use the process. Thus the claim invention has no concrete result.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Puri et al., U. S. Patent No. 6018621).

4. As to claims 1, 8, 13, and 14 Puri et al. teach a method of designing a logic circuit to provide a predetermined logical operation, the method including the steps of: (a) defining a logic synthesis block comprising a single dynamic logic circuit (as specification define dynamic logic is synthesis block (see fig 1, fig 2 col 1 line 20-52, and fig 7, fig 8 and col 6 lines 55 to col 7 lines 53); (b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block (see fig 7-9 col 7 line 35 to col 9 line 25); (c) eliminating unused devices in the intermediate circuit to produce a final circuit (see fig 6-7 col 6 lines 1 to col 6 lines 54); and (d) sizing the devices in the final circuit (see fig 6-7 col 6 lines 1 to col 6 lines 54).

5. As to claim 2, 9, and 15 Puri et al. teach wherein the step of defining the logic synthesis block includes selecting the largest practical dynamic AND/OR circuit for the integrated circuit fabrication technology in which the circuit is to be implemented (see fig 4-10 col 5 lines 35 to col 6 lines 15).

6. As to claim 3, 10, and 16 Puri et al. teach wherein the logic synthesis block comprises a four high and four wide dynamic AND/OR circuit (see fig 5a-5f and fig 6 and col 3 lines 41 to col 4 lines 51, and summary).

7. As to claim 4, 11, and 17 Puri et al. teach wherein the step of performing logic synthesis includes leaving the size of the devices in the logic synthesis block substantially unconstrained (see fig 7-9 col 7 line 35 to col 9 line 25).

8. As to claim 5, Puri et al. teach wherein the step of eliminating unused devices from the intermediate circuit includes detecting devices having a state that remains constant as the intermediate circuit operates to provide the predetermined logical operation (see fig 6-7 col 6 lines 1 to col 6 lines 54, and background).

9. As to claim 6, Puri et al. teach wherein the step of sizing the devices in the final circuit includes analyzing the final circuit to determine the characteristics of each device in the final circuit necessary in order to consistently provide the predetermined logical operation and meet drive requirements (see fig 6-7 col 6 lines 1 to col 6 lines 54, and background).

10. As to claim 7, 12, and 18 Puri et al. teach wherein the logic synthesis block uses a single activation/reset clock signal (see fig 1, fig 2 col 1 line 20-52, and fig 7, fig 8 and col 6 lines 55 to col 7 lines 53).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
May 12, 2007

05/12/07

THUAN V. DO
PRIMARY PATENT EXAMINER